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BLOCK DISTORTION DETECTION APPARATUS, BLOCK DISTORTION  
DETECTION METHOD AND VIDEO SIGNAL PROCESSING APPARATUS

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#### TECHNICAL FIELD

The present invention relates to a block distortion  
detection apparatus and a block distortion detection  
method for detecting a block distortion in an analogue  
10 video signal caused by block encoding of an image, and a  
video signal processing apparatus.

#### BACKGROUND ART

Conventionally, as an encoding method for  
15 effectively performing compression encoding on still  
image data and motion data, block DCT (discrete cosine  
transformation) encoding and other block encoding are  
known.

At the time of compression/decompression by such  
20 block encoding, a block distortion (block noise) may  
arise and the noise arises easier as the compression rate  
becomes high. The block distortion is an error of a  
reproduction data value at a boundary with an adjacent  
block recognized as noise because transformation is  
25 performed in a closed space in the DCT encoding, etc. and

continuity declines at the block boundary.

When data including the block distortion is converted to analogue data after that, it becomes harder to reduce the block distortion because there is no means  
5 for obtaining information on a location of the block boundary.

Conventionally, to solve the problem, for example, the Japanese Unexamined Patent Publication No. 2000-350202 (pp. 3 to 4, FIG. 1 and FIG. 2) proposes a  
10 technique of determining existence of a block distortion by outputting a differential signal based on an input luminance signal, detecting an isolated differential point from the differential signal, performing integration processing on the isolated differential point  
15 in accordance with a pixel block cycle, and cumulatively adding information on isolated differential points generated at the pixel block cycle.

In this method, however, block boundaries cannot be accurately discriminated from changes of a luminance  
20 signal in a scene with a greatly changing luminance signal. For example, an existence of a block distortion may be erroneously determined by detecting an isolated differential point in an image including much high frequency components, an image of a column, etc. and a  
25 pulsing noise, etc. and cumulatively adding the detected

isolated differential points.

Accordingly, when performing video signal processing based on the erroneously determined block boundaries, there is a problem that the image quality  
5 deteriorates.

#### DISCLOSURE OF THE INVENTION

An object of the present invention is to provide a highly accurate block distortion detection apparatus, a  
10 video signal processing apparatus and a block distortion detection method with minimum erroneous detection in a video signal, wherein information on block boundaries is lost.

To attain the above object, according to a first  
15 aspect of the present invention is a block distortion detection apparatus for detecting a block distortion occurred during block encoding of an image, comprising:  
an edge detection means for detecting an existence of an edge in each of a plurality of pixel signals based on  
20 differences of each of successive pixel signals; an edge count means including a plurality of counters, a number of which is determined in response to a number of pixels included in a block, for successively accepting and  
counting edge detection results of the edge detection  
25 means respectively by the plurality of counters at first

timing, which is synchronized with a horizontal  
synchronization signal; and a block boundary  
identification means for successively retrieving counter  
values of the plurality of counters at second timing,  
5 which is synchronized with a vertical synchronization  
signal, and for identifying a block boundary based on the  
counter values of the counters and an order of retrieving  
the edge detection results by the respective counters.

Also, to attain the above object, a second aspect  
10 of the present invention is a block distortion detection  
method for detecting a block distortion due to block  
encoding of an image, including the steps of detecting an  
existence of an edge in each of a plurality of pixel  
signals based on differences of the plurality of  
15 successive pixel signals; successively retrieving edge  
detection results of the edge determination means  
respectively by a plurality of counters in accordance  
with the number of pixels included in a block at first  
timing in synchronization with a horizontal  
20 synchronization signal and counting; and successively  
retrieving counter values of the plurality of counters at  
second timing in synchronization with a vertical  
synchronization signal and identifying as a block  
boundary based on an order of retrieving the edge  
25 detection results by the counters and a counter value of

the counters.

Also, to attain the above object, a third aspect of the present invention is a block distortion detection method for detecting a block distortion due to block encoding of an image, comprising an edge detection means for detecting an existence of an edge in each of a plurality of pixel signals based on differences of the plurality of successive pixel signals; an edge count means including a plurality of counters in accordance with the number of pixels included in a block, for successively retrieving edge detection results of the edge determination means respectively by the plurality of counters at first timing in synchronization with a horizontal synchronization signal and counting; a block boundary identification means for successively retrieving counter values of the plurality of counters at second timing in synchronization with a vertical synchronization signal and identifying as a block boundary based on an order of retrieving the edge detection results by the counters and a counter value of the counters; and a filtering means for performing filtering processing on the pixel signals at the block boundary position specified by the block boundary identification means.

According to the block distortion detection apparatus according to the first aspect of the present

invention, the edge detection means detects an existence of an edge in each of a plurality of pixel signals based on differences of the plurality of successive pixel signals. The edge count means includes a plurality of  
5 counters in accordance with the number of pixels included in a block, successively retrieves edge detection results of the edge determination means respectively by the plurality of counters at first timing in synchronization with a horizontal synchronization signal and counts. The  
10 block boundary identification means successively retrieves counter values of the plurality of counters at second timing in synchronization with a vertical synchronization signal and identifies as a block boundary based on an order of retrieving the edge detection  
15 results by the counters and a counter value of the counters.

Since the plurality of counters correspond respectively to horizontal positions on a screen, it is possible to quantitatively detect a horizontal position  
20 where a block distortion arises in accordance with counter values of the plurality of counters.

#### BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a block distortion  
25 detection apparatus according to a first embodiment.

FIG. 2 is a view of a circuit diagram of an edge detection circuit 2.

FIG. 3 is a view of a circuit diagram of an edge count circuit 3 and a boundary determination circuit 4.

5        FIG. 4 is a view for explaining edge determination processing in an edge determination circuit 24.

FIG. 5 is a view for explaining edge determination processing in an edge determination circuit 24.

10       FIG. 6 is a view for explaining edge determination processing in an edge determination circuit 24.

FIG. 7A to FIG.7C are timing charts for explaining an operation of a horizontal position setting counter 31.

FIG. 8A to FIG. 8D are timing charts for explaining operations of edge counters 34\_1 to 34\_16.

15       FIG. 9 is a block diagram of a video signal processing apparatus according to a second embodiment.

FIG. 10 is a block diagram of a video signal processing apparatus according to a third embodiment.

20       BEST MODE FOR CARRYING OUT THE INVENTION

#### First Embodiment

FIG. 1 is a block diagram of a block distortion detection apparatus 1 according to an embodiment of the present invention. As shown in FIG. 1, the block distortion detection apparatus 1 includes an edge

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detection circuit (EDGE) 2, an edge count circuit (E\_CNT) 3, a boundary determination circuit (BNRY) 4 and a filter (FIL) 5.

Note that the edge detection circuit 2, the edge count circuit 3 and the boundary determination circuit 4 are an embodiment of the edge detection means, the edge count means and the boundary determination means of the present invention, respectively.

The edge detection circuit 2 receives as an input a luminance signal Y and performs edge detection of the luminance signal Y based on a predetermined condition.

The edge count circuit 3 includes a plurality of counters and is configured that designated counter is switched for each pixel. The counter counts in order in accordance with an existence of an edge detected by the edge detection circuit 2.

The boundary determination circuit 4 rearranges values of the counters cumulated in the edge count circuit 3 in synchronization with a vertical synchronization signal, evaluates the same based on a predetermined condition and determines block boundaries.

When a boundary position of a block is determined in the boundary determination circuit 4, the filter 5 performs filtering processing on the luminance signal Y at the position. As shown in FIG. 1, a signal S5 after

the filtering processing is a video signal with reduced block distortion.

Below, respective components of the block distortion detection apparatus 1 will be explained in  
5 detail.

FIG. 2 is a block diagram of the edge detection circuit 2. As shown in FIG. 2, the edge detection circuit 2 is composed of a delay circuit 21, a computing unit 22, a computing unit 23\_1, a plurality of delay circuits 23\_2  
10 to 23\_7 and an edge determination circuit 24.

The delay circuit 21 gives a delay in an amount of one pixel sampling time to the input luminance signal Y. Therefore, a previous value of the luminance signal Y in the sampling in units of retrieved each pixels is held in  
15 the delay circuit 21.

The computing unit 22 calculates a difference of the previous value of the luminance signal T held in the delay circuit 21 and a present value of the currently input luminance signal Y.

20 The computing unit 23\_1 calculates an absolute value of the difference calculation of the previous value and present value of the luminance signal Y obtained in the computing unit 22. In FIG. 2, an output value of the computing unit 23\_1 becomes d1.

25 The delay circuits 23\_2 to 23\_7 give delay in an

amount of one pixel sampling time, respectively.

Therefore, the delay circuits 23\_2 to 23\_7 hold absolute values of differences of adjacent luminance signals Y respectively for input eight luminance signals Y in series. In FIG. 2, output values of the delay circuits 23\_2 to 23\_7 become d2 to d7, respectively.

The edge determination circuit (E\_JDG) 24 evaluates whether each pixel satisfies a later explained predetermined condition based on the output values d1 to d7 of the computing unit 23\_1 to 23\_7 and detects an existence of an edge. When an edge is detected, "1" is output, while when an edge is not detected, "0" is output.

Next, configurations of the edge count circuit 3 and the boundary determination circuit 4 will be explained.

FIG. 3 is a block diagram of the edge count circuit 3 and the boundary determination circuit 4. As shown in FIG. 3, the edge count circuit 3 includes a vertical position setting counter (CTR) 31, a counter switch 32, sixteen counter contacts 33\_1 to 33\_16 and sixteen edge time counters (CTR) 34\_1 to 34\_16.

The vertical position setting counter 31 is, for example, a four-bit counter and counts up in accordance with a sampling clock of the pixel and is reset at timing in synchronization with a vertical synchronization signal

of the image.

The counter switch 32 switches the counter contacts 33\_1 to 33\_16 in accordance with the horizontal position setting counter 31.

5       The edge time counters 34\_1 to 34\_16 are connected respectively to the counter contacts 33\_1 to 33\_16, and count an output signal 24S (1: an edge exists, 0: no edge) of the edge determination circuit 24 through the counters 33\_1 to 33\_16 set by the counter switch 32. Also,  
10       the counter values are reset at timing in synchronization with a vertical synchronization signal of the image.

Next, the configuration of the boundary determination circuit 4 shown in FIG. 3 will be explained. As explained in FIG. 3, boundary determination circuit 4  
15       includes a counter value sort unit (SORT) 41, a block boundary determination unit (B\_JDG) 42 and a time integration unit ( $\Sigma$ ) 43.

The counter value sort unit 41 is a register a register for holding counter values of the edge time  
20       counters 34\_1 to 34\_16 of the edge count circuit 3, respectively, and as shown in FIG. 3, retrieves the respective counter values of the edge time counters 34\_1 to 34\_16 at timing in synchronization with a vertical synchronization signal of the image. Furthermore, the  
25       counter value sort unit 41 rearranges the retrieved

respective counter values of the edge time counters 34\_1 to 34\_16 in an ascending order.

The block boundary determination unit 42 evaluates the counter values of the counter values of the edge time  
5 counters 34\_1 to 34\_16 rearranged in an ascending order in the counter value sort unit 41 based on a predetermined condition and determines a block boundary.

The time integration unit 43 performs time integration between fields of a predetermined image for  
10 the determination result of the block boundary determination unit 42, determines a block boundary position from the result and outputs existence of a block boundary and position information of the block boundary.

The respective components of the block distortion  
15 detection apparatus 1 were explained above.

Next, operations of the block distortion detection apparatus 1 including the above components as above will be explained in detail.

First, a video luminance signal Y is input to the  
20 delay circuit 21. The delay circuit 21 gives a delay corresponding to an amount of one pixel sampling to the input luminance signal Y and holds the data. Namely, the delay circuit 21 holds a previous value  $Y(n-1)$  of the previously input luminance signal.

25 Calculation of a difference of the currently input

luminance signal  $Y(n)$  for each pixel and the previous value  $Y(n-1)$  held in the delay circuit 21 in the computing unit 22, and  $Y(n) - Y(n-1)$  is obtained.

In the computing unit 23\_1, calculation of an absolute value of the difference calculation value  $Y(n) - Y(n-1)$  obtained in the computing unit 22 is performed to obtain  $|Y(n) - Y(n-1)|$ . Therefore,  $d1 = |Y(n) - Y(n-1)|$  here.

In the delay circuit 23\_2, a delay corresponding to an amount of one pixel sampling time to the absolute value  $|Y(n) - Y(n-1)|$  obtained in the computing unit 23\_1 and outputs to the delay circuit 23\_3. Accordingly,  $d2 = |Y(n) - Y(n-1)|$  stands. At the same time, in the computing unit 23\_1,  $d1 = |Y(n+1) - Y(n)|$  is obtained from  $Y(n)$  and the next luminous signal  $Y(n+1)$ .

Each of the delay circuits 23\_3 to delay circuit 23\_7 is set an output value of the previous delay circuit, gives a delay corresponding to an amount of one-time pixel sampling and outputs in the same way as the delay circuit 23\_2 does, so that an absolute value of a difference of adjacent luminance signals for each pixel is successively set to the delay circuits 23\_3 to delay circuit 23\_7 and output.

Note that it is obvious that the plurality of delay circuits explained above operate in synchronization with

a pixel sampling clock.

The edge determination circuit 24 determines for each pixel existence of an edge of the luminance signals on the output values d1 to d7 of the computing units 23\_1  
5 to 23\_7 operating as above.

Here, even if the difference absolute value of the luminance signal is a large value, it is necessary to prevent erroneous detection in the case of changes of luminance due to a video signal itself, such as a  
10 vertical line image of a column, etc., or one pulsing noise.

In FIG. 2, d4 is a luminance difference value (hereinafter, indicates an absolute value) for the edge determination and existence of an edge of the designated  
15 luminance difference value d4 is evaluated also in consideration of the previous and subsequent three values d1 to d3 and d5 to d7.

Here, by considering the points below, highly accurate detection of a block boundary becomes possible.

20 (1) In an image with greatly changing luminance, changes of the luminance may be erroneously determined as a block boundary, so that it is more accurate to detect a block boundary in the case of a luminance signal in a flat image, wherein luminance changes a little.

25 (2) Change of a level of block distortion is within

a certain range, so that erroneous determination with pulsing noise can be prevented by setting an upper limit of luminance changes.

Accordingly, the edge determination is performed by the three conditions below in the edge determination circuit 24.

Condition 1: There is not a large luminance signal difference value around a focused luminance signal difference value.

(Threshold A > d1) & (Threshold A > d2) & (Threshold A > d3) & (Threshold A > d5) & (Threshold A > d6) & (Threshold A > d7)

Condition 2: The focused luminance signal difference value is larger than an average of the surrounding luminance signal difference value at least by a multiple of 6/coefficient A.

$$d4 > (d1 + d2 + d3 + d5 + d6 + d7) / 6 \times (6 / \text{coefficient A})$$

$$\text{thus, } d4 > (d1 + d2 + d3 + d5 + d6 + d7) / \text{coefficient A}$$

(3) Condition 3: The focused luminance signal difference value is within a specific range.

$$\text{Threshold B} > d4 > \text{Threshold C}$$

Here, for example, values of A=16, B=40 and C=8 are applied to 10-bit luminance signal input.

Based on the above three conditions, how an actual

luminance signal is evaluated by the edge determination circuit 24 will be explained below by using FIG. 4 to FIG. 6.

FIG. 4 is an example of an image pattern, wherein a block distortion is visually conspicuous.

FIG. 5 is an example of an image pattern, wherein block distortion is not visually notable.

FIG. 6 is an example of an image pattern, wherein not a block distortion but a vertical line exists in every 8 pixels.

In FIG. 4 to FIG. 6, those indicated by a white circle and black circle are data of a luminance signal for each pixel and retrieved by the edge detection circuit 2, respectively. Here, seven difference values of adjacent luminance signals of eight black circles are set to the computing unit 23\_1 and the delay circuits 23\_2 to 23\_7.

Also, in FIG. 4 to FIG. 6, a difference of adjacent luminance signals is large in a portion sectionalized by lines L1 and L2. The part sectionalized by the line L1 is a currently focused luminance signal difference d1, and an existence of an edge at this part is evaluated based on seven luminance signal difference values including the previous and subsequent values.

In the image pattern in FIG. 4, a high frequency

part of the luminance signal is a little, a low frequency part accounts for a large part, and the block distortion is easily seen visually; so that it is an image pattern wherein an edge by the block distortion should be

5 detected. In FIG. 4, a part indicated as DC\_diff is a part to be a block distortion visually. In such an image pattern, it is unlikely to erroneously detect a block distortion, so that the above conditions 1 to 3 are set to perform edge detection caused by the block distortion.

10 Namely, since the luminous signal is a low frequency as a whole, luminance signal difference values other than the focused d4 are small and the condition 1 is satisfied. Also, an average value of the surrounding luminance signal difference values except for d4 is also  
15 small, so that it is considered to satisfy the condition 2.

If the d4 is not generated by a pulsing noise, it becomes a value in a predetermined range, so that the condition 3 is satisfied, so that an edge is detected at  
20 the d4 part in the image pattern in FIG. 4.

The image pattern in FIG. 5, the luminance signal has high frequency components, so that it is an image pattern, wherein the block distortion is not visually notable. In the image pattern as shown in FIG. 5, a block  
25 distortion itself is not notable and changes of the

luminance signal as a pattern of the image may be erroneously determined as a block distortion. The above conditions 1 to 3 are set so as not to perform edge detection in such a case.

5       Namely, any one of the luminance signal difference values d1 to d3 and d5 to d7 becomes larger than a predetermined threshold A, so that the condition 1 is not satisfied. Also, luminance signal difference values d1 to d3 and d5 to d7 around them becomes relatively large  
10 values, so that the average value also becomes large and the condition 2 may not be satisfied. If d4 is not caused by a pulsing noise, it becomes a value within a predetermined range and the condition 3 is satisfied.

Accordingly, edge detection is not performed at the  
15 d4 part in the image pattern in FIG. 5.

The image pattern in FIG. 6 has vertical lines existing in every 8 pixels in the luminance signal. Since the luminance signal difference value generated by the block distortion normally falls in a certain range, as  
20 shown in the image pattern in FIG. 6, the conditions 1 to 3 are set so that the edge detection is not performed when d4 is a large luminance signal difference value exceeding the certain range.

Namely, the luminance signal difference values d1  
25 to d3 and d5 to d7 around d4 become not larger than the

predetermined threshold A and satisfy the condition 1,  
and an average value of luminance signal difference  
values d1 to d3 and d5 to d7 around them also become  
small, so that the condition 2 is satisfied. However, in  
5 the condition 3, d4 exceeds a level of expected block  
distortion, so that the edge detection is not performed  
at the d4 part in the image pattern in FIG. 6.

As explained with reference to FIG. 4 to FIG. 6  
above, by setting the above conditions 1 to 3, the edge  
10 detection is not performed on an image pattern having a  
luminance signal having much high frequency components  
and an image including a vertical line or a pulsing noise,  
and the edge detection is performed only on a luminance  
signal, wherein high frequency components are a little  
15 and a block boundary is easily recognized, so that  
erroneous determination of the block boundary position  
can be reduced.

Naturally, it is possible to reduce erroneous  
determination of the block boundary position to a certain  
20 extent even when not all of the conditions 1 to 3 are set.

For example, when applying only the conditions 1  
and 2, erroneous determination may be made when the  
luminance signal includes a pulsing noise, but edge  
detection can be performed on a stable luminance signal  
25 not including high frequency components. Also, there is

an advantage that erroneous determination at least on a pulsing noise is not caused when the condition 3 alone is applied.

The edge determination circuit 24 outputs as a  
5 signal S24 as the edge determination result in FIG. 2 "1" only when all of the conditions 1 to 3 above are matched and outputs "0" in other cases.

Note that optimal values of the threshold A,  
threshold B, threshold C and coefficient A vary more or  
10 less depending on the configuration of a system on the previous stage of the block distortion detection apparatus 1, so that it is preferable that they can be set from the outside.

Next, a circuit operation of the edge count circuit  
15 3 will be explained by using FIG. 3.

First, the output signal S24 (edge exists: "1", no edge exists: "0") as the edge determination result is successively input in units of pixel sampling from the edge determination circuit 24 in the edge detection  
20 circuit 2 to the edge count circuit 3.

The horizontal position setting counter 31 counts up in units of pixels and the counter switch 32 switches connection positions of contacts successively, such as the counter contact 33\_1 → counter contact 33\_2 → ..., in  
25 accordance therewith. The horizontal position setting

counter 31 is reset at timing in synchronization with a video horizontal synchronization signal, so that the output signal S24 ("1" or "0") as the edge determination result is counted successively by the edge time counters  
5 34\_1 to 34\_16 by following the video horizontal position.

Counter values of the edge time counters 34\_1 to 34\_16 are reset at timing in synchronization with a video vertical synchronization signal, so that the above operation is performed for every field of an image.

10 Note that, as will be explained later on, a counter value immediately before resetting the counter value at timing in synchronization with the video vertical synchronization signal is retrieved by the boundary determination circuit 4 in an order that the edge time  
15 counter 34\_1 to 34\_16 retrieve the signal S24.

Here, the reason why the edge time counter is composed not by the number of 8 as a pixel interval to normally generate a block distortion but by the number of 16 as a multiple of 8 is that the possibility of  
20 erroneous detection is prevented by incidentally increasing only one counter value when a vertical line, such as a column, on a screen, so that performance of the block boundary detection is improved.

A method of evaluating the erroneous detection  
25 prevention performed in the boundary determination

circuit 4 will be explained later on.

FIG. 7A to FIG. 7 C are timing charts for explaining an operation of the horizontal position setting counter 31. In FIGS. 7, FIG. 7 A indicates a sampling clock CLK of pixels, FIG. 7 B indicates a horizontal synchronization signal H\_SYNC of an image, and FIG. 7C indicates a counter value H\_CTR of the horizontal position setting counter 31.

As shown in FIGS. 7, the counter value H\_CTR of the horizontal position setting counter 31 is counted up in synchronization with the sampling clock CLK of an image, and the counter value H\_CTR is reset at timing in synchronization with the horizontal synchronization signal H\_SYNC of the image. Accordingly, by resetting the counter value H\_CTR of the horizontal position setting counter 31 at timing in synchronization with the horizontal synchronization signal H\_SYNC of the image, it is determined to which counter in the edge time counters 34\_1 to 34\_16 the signal S24 ("1" or "0") as the edge detection result is retrieved in accordance with a position of the screen.

As explained above, edge detection results are count up in a counter group of the edge time counters 34\_1 to 34\_16 successively in units of pixel.

FIG. 8A to FIG. 8D are timing charts for explaining

operations of edge counters 34\_1 to 34\_16 performed at timing in synchronization with the vertical synchronization signal of the image. In FIGS. 8, FIG. 8A shows a sampling clock CLK, FIG. 8B shows a vertical synchronization signal V\_SYNC, FIG. 8C shows a counter values E\_CTR of the edge time counters 34\_1 to 34\_16, and FIG. 8D shows a register value SORT\_R of the counter value sort portion 41 in the boundary determination circuit 4, which will be explained later on.

10 In FIGS. 8, in the edge time counters 34\_1 to 34\_16, counter values E\_CTR are reset at timing in synchronization with the vertical synchronization signal V\_SYNC, and values CNTn immediately before the resetting are retrieved by the register of the counter value sort  
15 unit 41 in the boundary determination circuit 4, which will be explained later on.

The counter values E\_CTR of the edge time counters 34\_1 to 34\_16 are retrieved by the register of the counter value sort unit 41 in an order that the edge time  
20 counters 34\_1 to 34\_16 retrieved the signal S24 as the edge detection result. Accordingly, when assuming that the signal S24 as the edge detection result is retrieved in an order of, for example, the edge time counter 34\_1 → 34\_2 → ..., their counter values are retrieved to the  
25 counter value sort unit 41 of the boundary determination

circuit 4 in an order of S34\_1 → S34\_2 → ...

Next, an operation of the boundary determination circuit 4 will be explained with reference to FIG. 3.

In the counter value sort unit 41, as explained  
5 above, the counter values of the edge time counters 34\_1 to 34\_16 in the edge count circuit 3 are retrieved at timing in synchronization with a vertical synchronization signal of the screen and rearranged in an ascending order based on the counter values.

10 At that time, the respective counted values are retrieved to the counter value sort unit 41 in an order that the edge time counters 34\_1 to 34\_16 retrieved the signal S24 as the edge detection result, that is, in an order of switching by the counter switch 32. Furthermore,  
15 the counter value sort unit 41 rearranges respective counter values of the edge time counters 34\_1 to 34\_16 in an ascending order.

The rearranged counter value result is output to the block boundary determination unit 42 for a block  
20 boundary evaluation.

In the block boundary determination unit 42, the counter values set to the register and rearranged in the counter value sort unit 41 are evaluated to determine whether a block boundary is included between luminance  
25 signals in an amount of 16 pixels. By evaluating the

luminance signals in an amount of 16 pixels, a block distortion normally arises in every 8 pixels can be surely detected without an error.

For example, when a vertical line, such as a column,  
5 exists on a screen, the possibility of erroneous detection can be prevented as a result that only one counter value, so that performance of the block boundary detection can be improved. Also, there is an advantage of being able to deal with a block distortion arising in  
10 every 16 pixels easily when composed by 16 edge time counters.

The block boundary determination unit 42 determines that a block boundary is detected when the three conditions below are satisfied.

15

Condition 4: A difference is 8 in the order of retrieving counters having the largest and the second largest counter values by the counter value sort unit 41.

Condition 5: The second largest counter value is  
20 not less than the threshold D.

Condition 6: A ratio of the second largest counter value to the third largest counter value is not less than a predetermined ratio threshold E.

25 The above condition 4 takes consideration that a

block distortion arises in every 8 pixels in the case of a general MPEG2 signal, etc. For example, the counter switch 32 is switched by the horizontal position setting counter 31 at timing in synchronization with a horizontal synchronization signal of an image, so that an output value of the edge detection result is counted by the edge time counters 34\_1 to 34\_16 in an order of 34\_1 → 34\_2 → ... Since a counter value of the horizontal position setting counter 31 corresponds to a horizontal position on the screen, in the case where a block distortion arises in every 8 pixels, for example when the counter value of the edge time counters 34\_1 is a large number, the edge time counter 34\_9 for counting an edge at a position shifted by an amount of 8 pixels on the horizontal position also has a large counter value.

Accordingly, it is possible to determine a block distortion when a difference is 8 in the order that the counter value sort unit 41 retrieves the counters having the largest counter value and the second largest counter value rearranged in the register.

Also, in the case of a general block distortion, as explained above, it arises in 8 pixels, therefore, the second largest counter value also becomes large than a predetermined value.

Accordingly, by providing the above condition 5,

when an image including a vertical line, such as a column,  
and a pulsing noise are reflected to the counter value,  
only the largest counter value is a large value and the  
second largest counter value is not large, so that they  
5 can be taken out and the possibility of erroneously  
detecting a block distortion can be reduced.

Furthermore, as indicated in the above condition 1,  
the edge determination circuit 24 performs edge detection  
by focusing on a relatively flat part of the image, the  
10 largest and the second largest counter values are  
preeminent when a block distortion is detected and the  
third largest counter value and on become smaller  
comparing with them. In other cases, it is considered  
that a noise other than a clock distortion is counted and  
15 a block distortion may be erroneously detected.

Accordingly, when a ratio of the second largest  
counter value to the third largest counter value is a  
predetermined ratio or larger, a block distortion is to  
be detected. Namely, by adding the above condition 6, the  
20 possibility of erroneous detection can be reduced.

Note that, even when not all of the above  
conditions 4 to 6 are applied, the erroneous detection  
reduction effect of a block distortion is maintained to a  
certain extent. For example, even when only the condition  
25 4 is applied, the effect of detecting block distortions

arising in every 8 pixels is obtained and the possibility of erroneous detection of a block distortion becomes relatively low.

Note that it is preferable that the threshold D and  
5 the threshold E in the above conditions 5 and 6 can be set from the outside because the optimal values vary more or less due to the system configuration as same as the thresholds A to C explained above.

In the block boundary determination unit 42, based  
10 on the above three conditions 4 to 6, counter values of the edge time counters 34\_1 to 34\_16 are evaluated at timing of a vertical synchronization signal, and it is determined as a block boundary when the all three conditions are satisfied. The determination result is  
15 output to the time integration unit 43. For example, "1" may be output when it is determined to be a block distortion, while "0" in other cases in the same way as in the output signal S24 as an edge detection result.

When it is determined to be a block boundary, the  
20 block boundary determination unit 42 also outputs to the time integration unit 43 information on the block boundary position indicating that the block boundary is between which luminance signals. As explained above, the horizontal position corresponds to the order of counter  
25 values of the edge time counters 34\_1 to 34\_16 retrieved

by the counter value sort unit 41, so that each counter value can be made sequentially associated with the horizontal position.

In the time integration unit 43, when a block  
5 boundary is detected in the block boundary determination unit 42, time integration is furthermore performed for certain time based on the detection result.

When a block boundary position for each field as information from the block boundary determination unit 42  
10 indicates the same block boundary position for a predetermined time, for example from 2 fields to 4 fields, the time integration determines the position as the block boundary position. Namely, assurance of the block boundary position is improved by performing the time  
15 integration.

The time integration unit 43 outputs to the filter  
5 information on the identified block boundary position and filtering ON/OFF.

In the filter 5, filtering processing to reduce  
20 block distortion is performed only on around a luminance signal having a block distortion. As a result, quality of the image can be improved. Note that well known existing techniques can be applied.

As explained in the operation of the block  
25 distortion detection apparatus 1 above, the block

distortion detection apparatus 1 is provided with an edge detection circuit 2, an edge count circuit 3, a boundary determination circuit 4 and a filter 5, wherein the edge detection circuit 2 detects an edge based on a luminance signal difference in units of pixels. The edge count circuit 3 is provided with 16 counters, wherein the sixteen counters count detected edges at timing in synchronization with a horizontal synchronization signal of an image for each field in the image. In the boundary determination circuit 4, a block boundary is determined in accordance with the counting result, a block boundary position is determined by time integration of the determination result, and filtering processing is performed on a luminance signal in units of pixels at the determined block boundary position; so that the block distortion is reduced.

Note that the present invention is not limited to the explanation on the embodiments above and may be variously modified within the scope of the present invention.

In the above embodiments, a difference of input successive eight luminance signals was held in the computing unit 23\_1 and delay circuits 23\_2 to 23\_7 in the edge detection circuit 2, but the number is not limited to eight and it may be configured to store the

difference of the larger number, for example, successive sixteen of luminance signals.

When the luminance signals are input by an odd number, a difference to be stored becomes an even number  
5 and there are two luminance difference values to be focused as the middle value, so that one number is not determined but there arises no problem if which should be used is set in advance.

Also, when the computing unit 23\_1 and the delay  
10 circuit group are configured as such, it is needless to mention but the conditions 1 to 3, thresholds A to C and coefficient A for determination in the edge determination circuit 24 have to be reset based on the same concept.

Also, in the above embodiments, the edge time  
15 counters 34\_1 to 34\_16 are composed of sixteen counters, but the number is not limited to 16 as far as it is larger than 16 and multiples of 8. For example, when being composed of 24 edge counters, the determination conditions (the conditions 4 to 6) in the block boundary  
20 determination unit 42 may be set so as to furthermore reduce erroneous detection. Namely, even when there are two vertical lines in every 8 pixels, erroneous detection is not caused. In that case, it should be changed to evaluate the larger three counter values in the condition

When the edge time counter is composed, for example, of 24 counters, a change has to be naturally made on the horizontal position setting counter 31 in accordance therewith from 4 bits to 5 bits, etc.

5           In the above embodiments, the case of a luminance signal including a block distortion arising in every eight pixels was explained, but the number is not limited to 8 and the case with block distortions arising, for example, in 16 pixels may be also applied.

10           In that case, when assuming that the edge time counter 32 of the edge count circuit 3 is composed of counters by the number of 32 multiplied by an even number and the horizontal position setting counter 31 is, for example, a 6-bit counter, it becomes possible to detect  
15 an edge arising in every 16 pixels by the edge time counter.

Also, in the above embodiments, the horizontal position setting counter 31 of the edge count circuit 3 counts up in accordance with a timing of the pixel  
20 sampling clock, but the method is not limited to the counting-up way and the counting-down way from a predetermined initial value may be applied.

In that case, the determination conditions (conditions 4 to 6) in the block boundary determination  
25 unit 42 become as conditions 4' to 6' below.

Condition 4': A difference is 8 in the order of retrieving counters with the smallest and the second smallest counter values by the counter value sort unit 41.

5        Condition 5': The second smallest counter value is not larger than the threshold D.

Condition 6': When comparing the second smallest counter value and the third smallest counter value, it is not larger than a predetermined ratio threshold E.

10        Second Embodiment

Next, an embodiment of a video signal processing apparatus of the present invention will be explained.

FIG. 9 is a block diagram of a video signal processing apparatus according to the second embodiment.

15        As shown in FIG. 9, in the second embodiment, a video signal is distributed from a satellite broadcast (SAT) to, for example, to cable television (C\_TV) and analogue broadcast (ANG\_B) from the cable television (C\_TV) is received by a video signal processing apparatus  
20 100, such as a TV set, via a set-top box (BOX).

Here, the video signal distributed from the satellite broadcast SAT includes a block distortion due to block encoding of MPEG. Since a video digital signal including the block distortion is converted to analog by  
25 the cable television C\_TV, information on block

distortion boundary is lost.

The video signal processing apparatus 100 receives such an analog video signal including a block distortion in a form of an analog composite signal (CPS) and  
5 performs processing.

As shown in FIG. 9, the video signal processing apparatus 100 in the second embodiment includes an A/D converter (A/D) 110, a YC separator (YCS) 120 and a block distortion detection unit 130.

10 Below, an operation of the video signal processing apparatus 100 will be explained based on FIG. 9.

The A/D converter 110 receives as an input an analog composite signal (CPS) including a block distortion, performs A/D conversion and supplies a  
15 digital signal S110 to the YC separator 120.

The YC separator 120 receives as an input a digital composite signal S110 and performs YC separation. A separated video luminance signal is supplied as a signal S120 to the block distortion detection unit 130.

20 In the A/D converter 110 and YC separator 120, a block distortion is not removed from the analog composite signal (CPS) input to the video signal processing apparatus 100.

The block distortion detection unit 130 receives as  
25 an input the video luminance signal S120 separated in the

YC separator 120, detects a block distortion, and performs filtering processing on the input video luminance signal in accordance with the detected block distortion.

5           The configuration and operation of the block distortion detection unit 130 are the same as those in the block distortion detection apparatus 1 explained in the first embodiment. Accordingly, the block distortion included in the analog video signal input to the video  
10   signal processing apparatus 100 is reduced.

#### Third Embodiment

Next, a video signal processing apparatus according to a third embodiment will be explained.

FIG. 10 is a block diagram of a video signal  
15   processing apparatus according to the third embodiment. As shown in FIG. 10, in the third embodiment, a video signal processing apparatus, such as a TV set, receives a video signal of, for example, a DVD player and a video CD as an analog component signal CMP or an analog composite  
20   signal CPS.

Here, the video signal from a DVD player or video composite is an analog composite signal CPS or analog component signal (CMP) including a block distortion due to block encoding of MPEG, wherein information on the  
25   block boundary is already lost.

As shown in FIG. 10, the video signal processing apparatus 100a in the third embodiment includes an A/D converter (A/D) 110a, a YC separator (YCS) 120a and a block distortion detection 130a.

5       The respective components of the video signal processing apparatus 100a correspond to the A/D converter (A/D) 110, YC separator (YCS) 120 and block distortion detection 130, and the operations are same, thus the block distortion included in the analog video signal  
10   input to the video signal processing apparatus 100a is reduced.

Note that in the operation of the video signal processing apparatus 100a, it is needles to mention but YC separation by the YC separator 120a is not performed  
15   when the input signal is an analog component signal CMP.

As explained above, the video signal processing apparatuses according to the second and third embodiments receive analog video data including a block distortion and detect the block distortion based on a video  
20   luminance signal subjected to A/D conversion and, furthermore, in accordance with need, a video luminance signal obtained from the YC separator.

The configuration and operations of the block distortion detection units 130 and 130a are the same as  
25   those in the block distortion detection apparatus 1

according to the first embodiment. As a result, high quality image, wherein erroneous determination of a block boundary position is reduced, can be obtained.

#### Industrial Applicability

- 5       The present invention can be applied to a video reproducing apparatus for reproducing block encoded image data, etc.